CLAIMS

What is claimed is:

1. A method of trench formation within a dielectric layer, comprising:

first, etching a via within said dielectric layer, said via having a first depth;

second, depositing an organic plug layer within said via;

third, etching a trench with a first gas mixture to a second depth, said second depth being less than said first depth; and

fourth, further etching said trench with a second gas mixture to a third depth, said third depth being greater than said second depth and less than said first depth.

2. The method of claim 1 further comprising providing an intermediate layer between said via and said trench, said intermediate layer being at said third depth.

3. The method of claim 1 wherein said dielectric layer has a metallized object beneath the dielectric layer separated by a barrier layer, the method including a fifth etching step of etching through said barrier layer to the metallized object.

4. The method of claim 1 applied to the formation of a via-first dual damascene structure on a wafer further comprising, depositing a hardmask on said dielectric prior to etching a via within said dielectric layer that identifies identifies the location of said via with said hardmask.

5. The method of claim 1 wherein said dielectric layer is a low-k material having a k value of less than 3.0.

6. The method of claim 5 wherein said dielectric layer is an organosilicate glass dielectric.

7. The method of claim 1 wherein said first gas mixture is a polymerized gas mixture.

8. The method of claim 7 wherein said polymerized gas mixture includes a fluoro-carbon gas.

9. The method of claim 7 wherein said polymerized gas mixture includes a hydro-fluoro-carbon gas.

10. The method of claim 7 wherein said second gas mixture is a non-polymerized gas mixture.

11. The method of claim 10 wherein said non-polymerized gas mixture includes NF_3.

12. The method of claim 10 wherein said non-polymerized gas mixture include CF_4.

13. A method of trench formation within a low-k dielectric layer without an intermediate etch-stop layer, comprising:

first, etching a via within said dielectric layer, said via having a first depth;

second, etching a trench with a first gas mixture to a second depth, said second depth being less than said first depth; and

third, etching said trench with a second gas mixture to a third depth, said third depth being greater than said second depth and less than said first depth.

14. The method of claim 13 wherein said first gas mixture is a polymerized gas mixture.

15. The method of claim 14 wherein said second gas mixture is a non-polymerized gas mixture.

16. The method of claim 15 wherein said low-k dielectric layer has a k value of less than 3.0.

17. The method of claim 15 wherein said low-k dielectric layer is an organosilicate glass dielectric.

18. The method of claim 15 wherein said low-k dielectric layer has a metallized object beneath said low-k dielectric layer separated by a barrier layer, the method including a fifth etching step of etching through said barrier layer to said metallized object.

19. The method of claim 15 applied to the formation of a via-first dual damascene structure on a wafer further comprising, depositing a hardmask on said low-k dielectric prior to etching a via within said low-k dielectric layer that identifies the location of the said via with said hardmask.

20. An interconnect structure, comprising:

a low-k dielectric without an intermediate etch-stop layer;

a trench having a plurality of trench edges, said plurality of trench edges having a substantially orthogonal shape, said trench having a first width and a first depth within said low-k dielectric;

a via beneath said trench and within said low-k dielectric, said via having a plurality of via edges, said plurality of via edges having a substantially orthogonal shape, said via having a second width and a second depth, said second width being smaller than said trench first width and second depth being greater than said trench first depth.

21. The interconnect structure of claim 20 further comprising a terrace between said trench and said via, said terrace having a third width that is greater than said second via width.

22. The interconnect structure of claim 20 further comprising a metallized object beneath said via.

23. The interconnect structure of claim 21 further comprising a metallized object beneath said via.

24. The interconnect structure of claim 20 wherein said interconnect structure is a dual damascene structure.